Integrated 2.4 GHz CMOS Quadrature VCO with Symmetrical Spiral Inductors and Differential Varactors

Baoyong Chi and Bingxue Shi

Institute of Microelectronics, Tsinghua University, Beijing, 100084, China

Abstract **— A 2.4 GHz CMOS quadrature VCO is presented. By using symmetrical inductors and differential varactors, the circuit has been integrated into a single chip completely. The principles of this VCO are described. A prototype is fabricated in 0.25 um single-poly five-metal CMOS standard digital process. The measured results show that the proposed VCO could generate quadrature LO signals with a tuning range of more than 300 MHz and phase noise –104.33 dBc/Hz at 600 KHz offset@2.41 GHz (when only one port of differential outputs is measured). It consumes 21 mA when VDD=2.5 V (Including 8 mA output buffers). Die area is only 0.83x0.68 mm². This VCO could be used in many integrated wireless transceivers.**

I. INTRODUCTION

Recently, many transceivers incorporate quadrature-downconversion mixers due to its merits.[1~2] In the design of these transceiver systems, a major challenge is the generation of quadrature local oscillating (LO) signals. From system views, it requires quadrature LO signals to have high phase accuracy, good gain matching and low phase noise.[3] So far, there have been many methods proposed to generate quadrature LO signals. Among them, RC phase shift network and poly-phase network methods have restrictions in phase accuracy and gain matching due to the inaccuracies in actual values of R and C, and the noise performance and driving capability is not good.[4] Positive- and negative- edge triggered flip-flop method requires the oscillator and the flip-flop to work in double carrier frequency which aren't easy to design in radio frequency range.[5] Another method is to use even-stage voltage-controlled ring oscillator, but its phase noise performance is bad.[6] In [8,9], LO oscillators with quadrature outputs are proposed, but the performances of the circuits are limited by the LC tank components and the phase noise performance is little considered.

In this paper, a 2.4 GHz CMOS quadrature VCO is presented. It combines the LC-VCO, based on on-chip symmetrical spiral inductors and differential varactors, and two-stage ring VCO, similar to [9]. The principles of this VCO are described. A prototype is fabricated in 0.25 um single-poly five-metal CMOS digital process. The measured results show that the proposed VCO could generate quadrature LO signals with a tuning range of more than 300 MHz and phase noise –104.33 dBc/Hz at 600 KHz offset@2.41 GHz (when only one port of differential outputs is measured). It consumes 52.5 mW when VDD=2.5 V (Including 20 mW output buffers). Die area is only 0.83x0.68 mm². This VCO could be used in many integrated wireless transceivers.

The remainder of this paper is organized as follows. Section 2 contains the detailed description of the proposed VCO. The measured results are given in section 4. The final section offers some conclusions.

II. DESIGN DESCRIPTION

The schematic diagram of the proposed VCO is shown in Fig.1. M0 is a tail current source controlled by the bias voltage V_{BLO}, C0 is a large tail capacitor which provides a low impedance path to ac ground for higher harmonics, so it attenuates the high frequency noise component of the tail current source and improves the phase noise performance of the whole VCO. The cross-coupled p-MOSFET differential pairs M1~M4, in positive feedback, feed the LC tanks to compensate the loss.

Their transconductances are designed as follows:

$$g_m = 2G_m = 6/R_p = 6/\omega_0 L Q_{tank} \quad (1)$$

in which Gm is the transconductance of the cross-coupled active pairs, R_p is the parallel resistance of the LC tanks at resonance, ω_0 is the resonance frequency, L is the inductance of the LC tanks, Q_{tank} is the quality factor of the LC tanks. LC tank is based on on-chip symmetrical spiral inductor and differential varactors.[7] Fig.2 shows the symmetrical inductor's layout and the cross section of the differential varactor. These differential structures improve the tank's quality factor, reduce chip area, and improve the symmetry of the circuit, all these will lower flicker noise upconversion.

The n-MOSFETs M5~M8 compose a two-stage differential ring oscillator. The outputs of each stage are 90° out of phase.[9] By combination of the ring oscillator

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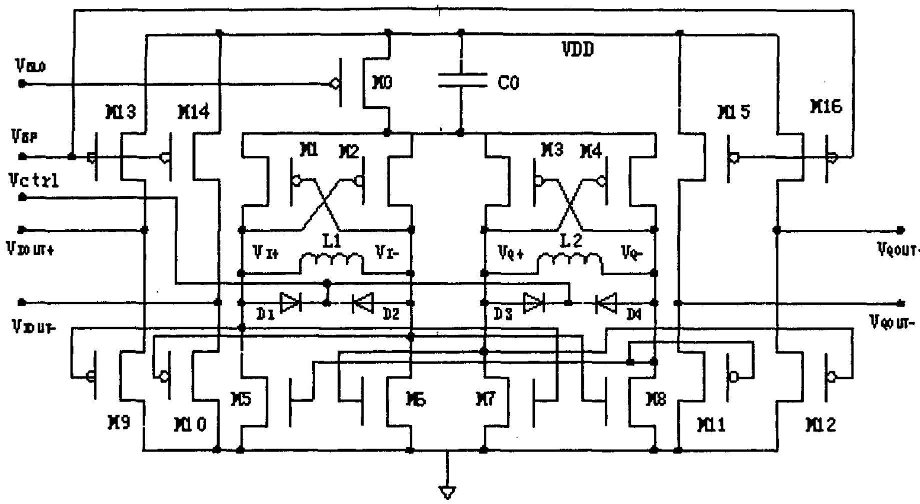
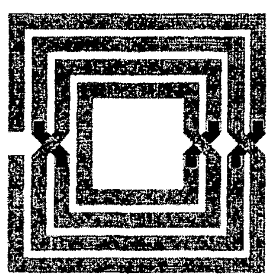
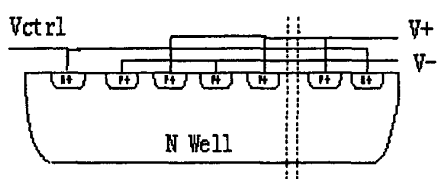


Fig. 1 Schematic diagram of quadrature VCO

and LC-VCO, the low phase noise quadrature LO signals could be got. The constant current source M0, shared by the two sections, further enhance the accuracy of the quadrature VCO.



(a)



(b)

Fig.2 (a) Symmetrical spiral inductor layout;

(b) The cross-section of the differential varactors

The p-MOSFETs M9~M16 compose four source followers, their roles are to drive the off-chip low impedance loads and to provide isolation. If the VCO is applied on a system on chip, these followers could be omitted.

III. MEASURED RESULTS

Before fabrication, the proposed circuit was simulated with HSPICE, using BSIM3.1 (Level 49) transistor models. The process provides 5 metal layers and 1 polysilicon layer. The symmetrical spiral inductors use the top metal layer. A CAD analysis and simulation tool of inductors, ASITIC,[10] is used to optimize the inductors and to extract the parasitic component parameters. Each inductor is realized with an inductance 4.16 nH, a quality factor 6.539 and an area $0.24 \times 0.24mm^2$. The symmetrical spiral inductors are also fabricated, and the measurements are done. The measured inductance value is 3.96 nH and the series resistance is 6.49Ω at 1MHz. Although the behavior in radio frequency rang is differential from the one in low frequency, but this measured results could be used as a basis to design the quadrature VCO.

Each diode is modeled by HSPICE Level 3 Diode model and a low series resistance. By layout strategy, the series resistance of each diode is lower to 0.52 Ω.

To find the quadrature performance of the outputs, the transient simulations and FFT analysis were done under 1% mismatch of the inductors and diodes. Table 1 lists the experimental results. It could be seen from Table 1 that the maximum phase error is less than $2.1°$ and the amplitude rate is less than 1.01 when the mismatchs of the inductors and the varactors are both 1%.

TABLE 1
EFFECT OF THE MISMATCHED DEGREE OF THE LC TANK COMPONENTS ON THE PHASE ACCURACY AND GAIN MATCHING

	Vctrl = 1.25 V *f* = 2.445 GHz			
Mismatched Degree	L: 0 C: 0	L:1% C:1%	L: 1% C: 0	L: 0 C:1%
Core phase error : *VI~VQ*	0.003	2.09	1.22	0.87
Output phase error : *VIOUT~VQOUT*	0.000	2.06	1.20	0.85
Core amplitude rate : *VI/VQ*	1.000	1.009	1.004	1.006
Output amplitude rate: *VIOUT/VQOUT*	1.000	1.011	1.004	1.006

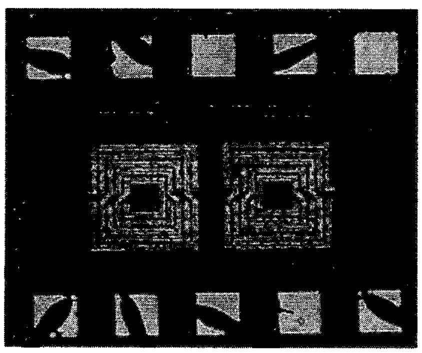


Fig.3 Microphotograph of the fabricated VCO

To verify the performance of the quadrature VCO, the proposed circuit has been fabricated in 0.25 um single-poly five-metal N-well 2.5 V CMOS digital process. Fig.3 shows the microphotograph of the fabricated VCO. The die size is $0.83 \times 0.68 mm^2$. A significant portion of the die is occupied by the pads and two inductors, and the core circuit area is only $0.62 \times 0.41 mm^2$.

Experimentally measured VCO transfer function is showed in Fig.4. When the control voltage changes from 0.8 V to 3.5 V, the oscillation frequency changes from 2.160 GHz to 2.465 GHz. So more than 300 MHz tuning rang could get. This is a very wide frequency rang and could satisfy many kinds of applications.

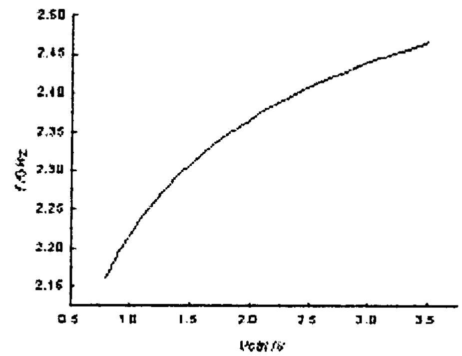


Fig.4 Experimentally measured VCO transfer function

The phase noise is –104.33 dBc/Hz at 600 KHz offset @2.41 GHz as shown in Fig.5. The measurement is done on one port of the differential outputs to reduce package pins. If differential outputs are drawn out, the measured phase noise would be more than 6dBc better. This could be explained as follows: when the measurements are done on the differential output, the oscillation amplitude would be 2 times larger. According to [11,12], the phase noise would be 6 dBc better; and differential outputs could reduce common-mode noise, so the phase noise would be more than –110.33 dBc/Hz at 600 KHz offset @2.41 GHz better if the different outputs are utilized. This result is very similar to the simulated result.

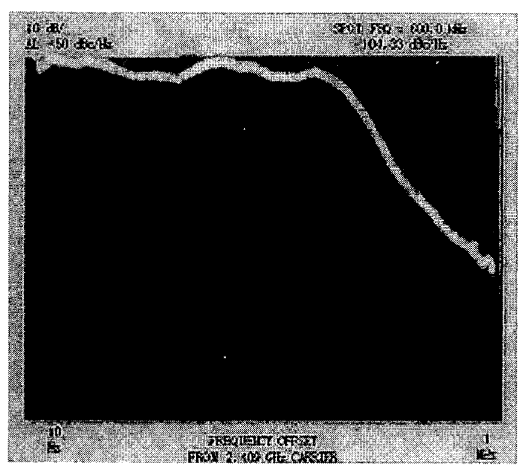


Fig.5 Measured phase Noise performance on one port of differential outputs

With the power supply voltage 2.5 V and the oscillation frequency 2.36 GHz, the total supply current is only 21 mA (four buffers consume 8mA) and the total power consumption is only 52.5 mW (four buffers consume 20mW). So each LC-VCO only consumes less than 26.3 mW (including two buffers), which is very power efficient.

IV. CONCLUSIONS

A 2.4GHz quadrature VCO is proposed. It could generate quadrature LO signals with high phase accuracy and good gain match under low power, good phase noise and small area, thus it could be used in many integrated transceivers.

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